What is claimed is:

1. A test circuit that is incorporated in a device having an output circuit for outputting a signal, and that carries out a verification of a connection of nodes of said device, said test circuit comprising:

a test data generating circuit generating test data for carrying out a verification of a connection of output nodes of said output circuit; and

a test output buffer, connected in parallel with said output nodes, receiving test data from said test data generating circuit and outputting the test data to said output nodes.

2. The test circuit as claimed in claim 1, wherein said output circuit outputs a differential signal, and said test output buffer outputs said test data to said differential output nodes.

3. The test circuit as claimed in claim 2, wherein said test circuit carries out the verification of the connection of said output nodes in a differential signal status.

4. The test circuit as claimed in claim 1, further comprising ESD protectors connected between said output nodes and said test output buffers.

5. The test circuit as claimed in claim 1 wherein, when said output circuit has a function of converting parallel data into serial data, said test data generating circuit also has a function of converting parallel data into serial data.

6. The test circuit as claimed in claim 1, wherein said test data generating circuit is constructed of a circuit that has a register function capable of performing scanning.

7. The test circuit as claimed in claim 1, wherein a test clock, which is different from an operation clock of said output circuit, is supplied to said test data generating circuit.

8. The test circuit as claimed in claim 1, wherein

said test data generating circuit outputs test data which is fixed to the verification of the connection of said output nodes.

9. The test circuit as claimed in claim 1, wherein an output of said output circuit is provided with a terminating resistor.

10. The test circuit as claimed in claim 1, wherein said test output buffer directly controls said output circuit.

11. The test circuit as claimed in claim 1, further comprising a test input buffer connected in parallel with input nodes of an input circuit to which a signal is applied, and said test input buffer receiving test data that are input to said input nodes.

12. The test circuit as claimed in claim 1, further comprising ESD protectors connected between said input nodes and said test input buffers.

13. The test circuit as claimed in claim 11, wherein said input circuit receives a differential signal, and said test input buffer receives test data that has been input to said differential input nodes.

14. The test circuit as claimed in claim 13, further comprising:

a circuit converting test data that has been input to said differential input nodes into a single end signal; and

a test data processing circuit processing said test data.

15. The test circuit as claimed in claim 14 wherein, when said input circuit has a function of converting serial data into parallel data, said test data processing circuit also has a function of converting serial data into parallel data.

16. The test circuit as claimed in claim 14, wherein said test data processing circuit is constructed of a specific circuit that has a register function capable of performing scanning.

17. The test circuit as claimed in claim 16, wherein said specific circuit having said register function has a test terminal.

18. The test circuit as claimed in claim 14, wherein a test clock, which is different from an operation clock of said input circuit, is supplied to said test data processing circuit.

19. The test circuit as claimed in claim 14, wherein said test data processing circuit processes test data which is fixed to the verification of the connection of said input nodes.

20. The test circuit as claimed in claim 1, wherein said test circuit carries out a JTAG test of a device in which a single end terminal and a differential terminal coexist.

21. A semiconductor integrated circuit device having an output circuit transmitting a signal, and a test circuit carrying out a verification of a connection of nodes, said test circuit comprising:

a test data generating circuit generating test data for carrying out a verification of a connection of output nodes of said output circuit; and

a test output buffer, connected in parallel with said output nodes, receiving test data from said test data generating circuit and outputting the test data to said output nodes.

22. The semiconductor integrated circuit device as claimed in claim 21, wherein said output circuit outputs a differential signal, and said test output buffer outputs said test data to said differential output nodes.

23. The semiconductor integrated circuit device as claimed in claim 22, wherein said test circuit carries out the verification of the connection of said output nodes in a differential signal status.

24. The semiconductor integrated circuit device as claimed in claim 21, wherein said test circuit further comprises ESD protectors connected between said output

nodes and said test output buffers.

25. The semiconductor integrated circuit device as claimed in claim 21 wherein, when said output circuit has a function of converting parallel data into serial data, said test data generating circuit also has a function of converting parallel data into serial data.

26. The semiconductor integrated circuit device as claimed in claim 21, wherein said test data generating circuit is constructed of a circuit that has a register function capable of performing scanning.

27. The semiconductor integrated circuit device as claimed in claim 21, wherein a test clock, which is different from an operation clock of said output circuit, is supplied to said test data generating circuit.

28. The semiconductor integrated circuit device as claimed in claim 21, wherein said test data generating circuit outputs test data which is fixed to the verification of the connection of said output nodes.

29. The semiconductor integrated circuit device as claimed in claim 21, wherein an output of said output circuit is provided with a terminating resistor.

30. The semiconductor integrated circuit device as claimed in claim 21, wherein said test output buffer directly controls said output circuit.

31. The semiconductor integrated circuit device as claimed in claim 21, wherein said test circuit further comprises a test input buffer connected in parallel with input nodes of an input circuit to which a signal is applied, and said test input buffer receiving test data that are input to said input nodes.

32. The semiconductor integrated circuit device as claimed in claim 21, wherein said test circuit further comprises ESD protectors connected between said input nodes and said test input buffers.

33. The semiconductor integrated circuit device as claimed in claim 31, wherein said input circuit receives a differential signal, and said test input buffer

receives test data that has been input to said differential input nodes.

34. The semiconductor integrated circuit device as claimed in claim 33, wherein said test circuit further comprises:

a circuit converting test data that has been input to said differential input nodes into a single end signal; and

a test data processing circuit processing said test data.

35. The semiconductor integrated circuit device as claimed in claim 34 wherein, when said input circuit has a function of converting serial data into parallel data, said test data processing circuit also has a function of converting serial data into parallel data.

36. The semiconductor integrated circuit device as claimed in claim 34, wherein said test data processing circuit is constructed of a specific circuit that has a register function capable of performing scanning.

37. The semiconductor integrated circuit device as claimed in claim 36, wherein said specific circuit having said register function has a test terminal.

38. The semiconductor integrated circuit device as claimed in claim 34, wherein a test clock, which is different from an operation clock of said input circuit, is supplied to said test data processing circuit.

39. The semiconductor integrated circuit device as claimed in claim 34, wherein said test data processing circuit processes test data which is fixed to the verification of the connection of said input nodes.

40. The semiconductor integrated circuit device as claimed in claim 21, wherein said test circuit carries out a JTAG test of a device in which a single end terminal and a differential terminal coexist.

41. A test circuit that is incorporated in a device having an input circuit for inputting a signal, and that carries out a verification of a connection of nodes of

said device, said test circuit comprising:

a test data generating circuit generating test data for carrying out a verification of a connection of input nodes of said input circuit; and

a test input buffer, connected in parallel with said input nodes, receiving test data from said test data generating circuit and inputting the test data to said input nodes.

42. The test circuit as claimed in claim 41, further comprising ESD protectors connected between said input nodes and said test input buffers.

43. A semiconductor integrated circuit device having an input circuit transmitting a signal, and a test circuit carrying out a verification of a connection of nodes, said test circuit comprising:

a test data generating circuit generating test data for carrying out a verification of a connection of input nodes of said input circuit; and

a test input buffer, connected in parallel with said input nodes, receiving test data from said test data generating circuit and inputting the test data to said input nodes.

44. The semiconductor integrated circuit device as claimed in claim 43, wherein said test circuit further comprises ESD protectors connected between said input nodes and said test input buffers.